IN THE SPECIFICATION:

Please amend the specification at page 7, lines 18-24 as follows.

Reference is now made to Figure 4, which is a logic diagram showing the architecture of the conversion circuit or interface 30. It comprises a first logic circuit L1 which receives the PWM signal as an input, and which has an output that delivers a zeroing signal RAZ. The way in which this zeroing signal is used will be seen later herein. The same output also delivers an error signal ERR which will also be used in a manner to be described later.